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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,247	03/23/2004	Naoto Horiguchi	042261	1770

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,247	NAOTO HORIGUCHI	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *8-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/01/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse of Group II (claims 1-7) in the reply filed on 9/6/05 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeuchi (U.S. 5,641,696).

As to claim 1, Takeuchi discloses in figures 4A-4B a method for manufacturing a semiconductor device comprising the steps of: forming a gate (12) over a semiconductor region ("semiconductor substrate" 10); forming a first junction (20) by doping an n-type impurity less diffusive than phosphorus in the semiconductor region (10) (see col. 13, lines 12-43) by using the gate (12) as a mask (col. 16, lines 37-44); and forming a second junction (19) by doping an n-type impurity in the semiconductor region (10) by using at least the gate (12) as a mask (col. 16, lines 37-44), the second junction (19) being deeper than the first junction (20), the second junction (19) overlapping with the first junction (20) with leaving a part of the first junction (20) existing under the gate (12), wherein the step of forming the first junction (20) includes at least a first ion implantation (col. 10, lines 38-42) which is carried out with a first acceleration energy ("30 Ke V)" and a first dose, and a second ion implantation ("second concentration") which is carried out with a second acceleration energy higher than the first acceleration energy ("30 Ke

V") and a second dose lower than the first dose ("second concentration lower than the first predetermined concentration") (see col. 10, lines 38-42).

As to claim 2, Takeuchi discloses in figures 4A-4B a method for manufacturing a semiconductor device, wherein in the step of forming the first junction (20), arsenic is used as the less diffusive n-type impurity ("low-concentration impurity") (col. 9, lines 10-12; col. 10, lines 42-61; and col. 13, lines 27-33).

As to claim 4, Takeuchi discloses in figures 4A-4B a method for manufacturing a semiconductor device, further comprising the step of forming side walls ("spacers" 15) over both sides of the gate (12), and wherein the step of forming the second junction (19) is carried out by using the gate (12) and the side walls ("spacers" or "side walls" 15) as a mask (col. 16, lines 37-44; and col. 21, lines 56-57).

As to claim 5, figure 11D of Takeuchi further comprising the step of processing the gate (12) to take the shape of a notch (gate 12 is shaped as a notch as shown in figure 11D), and wherein the step of forming the first junction (20) is carried out by using the gate (12) in the shape of the notch as a mask (see figure 11D; and col. 16, lines 37-44).

As to claim 6, Takeuchi discloses in figures 4A-4B a method for manufacturing a semiconductor device, further comprising the step of doping a p-type ("p sub" in figure 4A) impurity in the surface layer of the semiconductor region ("semiconductor substrate" 10) by using the gate (12) as a mask (col. 16, lines 37-44).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (U.S. 5,641,696) in view of Taka et al. (U.S. 4,853,342).

As to claim 3, Takeuchi does not disclose a step of forming the first junction includes a third ion implantation which is carried out with a third acceleration energy and a third dose, in addition to the first and second ion implantations.

Taka et al. disclose a step of forming the first junction includes a third ion implantation ("third ion-implantation") which is carried out with a third acceleration energy (40 KeV) and a third dose ($1.5x10^{11}$ cm^{-2}), in addition to the first and second ion implantations (see column 4, lines 13-15). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor substrate of Takeuchi by providing a third ion implantation in a semiconductor substrate as taught by Taka et al. for the purpose of providing a better n-type collector region on the entire substrate (see column 4, lines 5-7).

As to claim 7, Takeuchi does not disclose a second ion implantation is carried out with the acceleration energy of 20 keV to 30 keV and the dose of 1.times.10.sup.13/cm.sup.2 to 3.times.10.sup.13/cm.sup.2.

Taka et al. disclose a second ion implantation is carried out with the acceleration energy of 20 keV to 30 keV ("30 KeV") and the dose of 1.times.10.sup.13/cm.sup.2 to 3.times.10.sup.13/cm.sup.2. ("$1x10^{14}$ cm^{-2}") (see figures 1-2; column 4, lines 11-13; and column 5, lines 7-10). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor substrate of Takeuchi by having

the ion implantation which is carried out with the acceleration energy of 20 keV to 30 keV and the dose of 1.times.10.sup.13/cm.sup.2 to 3.times.10.sup.13/cm.sup.2 as taught by Taka et al. for the purpose of providing a desired carrier density distribution for the semiconductor device.

Response to Arguments

5. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gardner et al (U.S. 6,297,535), Yu (U.S. 6,506,650), Makabe et al (U.S. 2001/0028086), Talwar et al (U.S. 6,380,044), Makabe et al (U.S. 6,794,258), Tokushige et al (U.S. 2002/0068394), Wang et al (U.S. 5,776,811), Thurgate et al (U.S. 6,255,165), Huster (U.S. 6,238,978), and Lin et al (U.S. 6,297,098) disclose relevant prior arts.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
3 March 2006